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Attorney's Docket No.: 10559-165001 / P8249

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bryan R. White
Serial No. : 09/676,844
Filed : September 29, 2000
Title : SHARED TRANSLATION ADDRESS CACHING

Art Unit : 2676
Examiner : Mackly Moonestime

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Commissioner for Patents
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REPLY TO ACTION OF JUNE 10, 2004

(Assignee: Intel Corporation)

The applicant thanks the examiner for the interview held on August 10, 2004, in which claims 1, 7 and 13 and the reasons for the patentability of all of the claims were discussed. During the interview, the Examiner agreed to withdraw the finality of the June 10, 2004, Office Action, and to reconsider the patentability of the claims.

Each remark of the applicant below is preceded by a quotation of related comments of the Examiner, shown in bold small type.

3. Claims 1-3, 7-9 and 13 are rejected under 35 U. S. C. 103(a) as being unpatentable over Nielsen et al (US Patent No. 6,104,417) in view of Lohman (US Patent No. 6,714,957).

4. Nielsen et al were cited in the last office action.

5. As per claims 1 and 13, Nielsen et al substantially disclosed the invention as claimed, including a memory controller hub comprising: an internal graphics subsystem adapted to perform graphics operations on data (Fig. 2B; Item No. 218); determining whether the memory controller hub is operably coupled to an external graphics controller or performs graphics operations on data using internal graphics subsystem (Fig. 2B, Items No. 218, 210, 212).

Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and adapted to stored addresses of locations in physical memory available to an external graphics controller hub to store graphics data. However, Nielsen et al did disclose a rendering engine that supports a frame buffer address translation buffer (TLB) to translate frame buffer (x, y) addresses into physical memory addresses, wherein the TLB is loaded by CPU with the base physical memory addresses (Fig. 2B, Items No 208, 206). Moreover, the concepts and associated advantages of using a cache to store addresses of location physical memory; thus, as is well known in the art, both caches and buffers are often used in a similar manner (i.e. quick access to store data). Furthermore, Lohman